MERIDIAN Innovation

IC Layout Engineer

Job Description:

Meridian Innovation is recruiting an experienced IC layout engineer to be part of a highly talented group, to design state-of-the art Infrared Image Sensor ASIC. The candidate must have experience in mixed signal CMOS transistor level layout design. The candidate will perform low noise analog layout design, top level floor-planning and perform all LVS/DRC/ERC checks. Responsibilities include full-chip integration and physical verification sign-off.

Basic Qualifications

- Bachelors / Master degree in Electrical/Electronic/Computer Engineering
- Diploma holder with 5yrs+ experience will be considered.
- A self-motivated, creative, hard-working person with an entrepreneur mind set.
- Adaptability and willingness to learn new approaches, solutions and skills.
- Strong communication skills, problem solving and analytical skills.
- Strong knowledge in floor-planning techniques, power mesh planning, low noise signal routing, IO pads, ESD/LU and Mixed signal chip integration flow.
- Proficient in Cadence layout editor and physical verification tools.
- Proficient in DRC/LVS debugging.
- Knowledge in script programming, such as, Tcl, Perl or C-shell is a plus.
- Knowledge of place and route, static timing analysis and formal verification is a plus.
- Good knowledge of ADC, LNA, analog multiplexer, filter, bandgap is a plus.

Desired skills

- Work with other IC design engineers to implement top quality layout for optimized block level design.
- Work with other engineers to achieve full chip integration, physical implementation, tape out and testchip validation.
- Perform and pass all physical & reliability verification such LVC/DRC/ERC.
- Ensure the database is fully compliant with all requirements of tape-out flow.
- Responsible for Full-chip Physical Verification Sign-off.

Job Location(s): Singapore

Please contact Meridian Innovation (HK) LTD: hr@meridianinno.com